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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/654,315	09/03/2003	Michael P. Nesnidal	NGC-00087DA (11-0983D)	4373

7590 04/20/2004

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EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/654,315	NESNIDAL ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *03 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Under the heading "CROSS-REFERENCE TO RELATED APPLICATIONS", the Issued Patent Number US 6,649,439 resulting from the serial number 10/210, should be provided. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1 – 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zubrzycki, US 6,365,428.

Regarding claim 1, Zubrzycki teaches a method of making an optical diffraction device comprising:

- growing a first semiconductor layer 101 on a semiconductor substrate 100, said first semiconductor layer being made of semiconductor material having an index of refraction,
- depositing a layer 102 on the first semiconductor layer;
- patterning and etching the layer 102 to form openings in the layer 102 to expose selective areas on the first semiconductor layer 101 and to create diffraction regions made out of the material 102; and
- growing a second semiconductor layer 103 by an epitaxial growth process on the first semiconductor layer between the diffraction regions with reference to Fig. 1 and detail description of the process in between columns 3 and 4.

Zubrzycki fails to teach the layer 102 being a dielectric layer. However, Zubrzycki teaches that suitable dielectric layer can be deposited and etched to form surface gratings for the benefit of obtaining high contrast grating structures in column 2, lines 27 – 33.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Zubrzycki and replace the layer 102 with a dielectric layer

for the benefit of obtaining high contrast grating structures as taught by Zubrzycki in column 2, lines 27 – 33.

Regarding claim 2, Zubrzycki teaches growing the second semiconductor layer 103 to layer 104 that encloses the diffraction regions 102 with respect to Fig. 1 in column 4, lines 7 – 10.

Regarding claim 3, Zubrzycki teaches growing the second semiconductor layer layer 103 to layer 104 of the same GaAs material as that of layer 101 in between column 1, line 58 and column 4, line 10.

Regarding claim 5, Zubrzycki teaches growing a third semiconductor layer 104 over the second semiconductor layer 103 and the diffraction layer 102

6. Claims 4, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zubrzycki, US 6,365,428 in view of the Admitted Prior Art (APA) and Jannopoulos, US 5,955,749.

Regarding claim 4, Zubrzycki teaches growing the second semiconductor layer to be of same material but fails to teach growing the second semiconductor material of a different material having a different index of refraction.

The APA teaches that small difference in the index of refraction is needed for the benefit of enhancing the interaction of the optical modes in paragraphs 5 and 6.

Jannopoulos teaches forming the two semiconductor layers of different refractive indices with reference to Fig. 5 for the benefit of forming integrated light emitting devices in column 7, lines 47 – 67.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Zubrzycki and form the second layer of a different material having a different index of refraction for the benefit of enhancing the interaction of the optical modes as taught by the APA in paragraphs 5 and 6 and also for the benefit of forming integrated light emitting devices as taught by Jannopoulos in column 7, lines 47 – 67.

Regarding claim 6, Zubrzycki teaches growing the second semiconductor layer and a third semiconductor layer and the desirability of making high contrast grating structures having different indices of refraction in column 3, lines 28 – 45, but fails to teach that the third layer having higher index of refraction than that of the second layer.

The APA and Jannopoulos teach the desirability of having large difference of index of refraction as was described earlier in rejecting claim 5.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Zubrzycki and form the third layer of a different material having a different index of refraction than the second material for the benefit of enhancing the interaction of the optical modes as taught by the APA in paragraphs 5 and 6 and also for the benefit of forming integrated light emitting devices as taught by Jannopoulos in column 7, lines 47 – 67. Note that Zubrzycki's diffracting grating is also made in the semiconductor layer 102.

Regarding claim 7, Zubrzycki teaches that suitable dielectric layer can be deposited and etched to form surface gratings with air as a grating medium for the benefit of obtaining high contrast grating structures in column 2, lines 27 – 33.

7. Claims 8 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zubrzycki, US 6,365,428 in view of Scherer, US 6,468,823.

Regarding claim 8, Zubrzycki teaches a method for making an optical diffraction device comprising:

- growing a first semiconductor layer on a semiconductor,
- depositing a dielectric layer on the first semiconductor layer opposite to the substrate,
- patterning and etching the dielectric layer to form openings in the dielectric layer to expose selective areas on the first semiconductor layer and to create diffraction regions made out of the dielectric material, where the dielectric diffraction regions are spaced apart dielectric strips 24 as shown in Fig. 6,
- growing a second semiconductor layer by an epitaxial growth process on the first semiconductor layer between the dielectric diffraction regions so that the second semiconductor layer completely encloses the dielectric diffraction regions as was described earlier in rejecting claims 1 – 7.

Zubrzycki teaches forming gratings formed with air, but fails to teach etching access vias through the second semiconductor layer to expose the dielectric diffraction regions and etching away the diffraction region material to define the diffraction regions out of air.

Scherer teaches a method of producing optical devices in which he teaches etching access vias through the second semiconductor layer to expose the dielectric diffraction regions and etching away the diffraction region material to define the

diffraction regions out of air with reference to Figs 4, 5A, 5B and 6 and associated descriptions in columns 3 and 4 for the benefit of producing nanocivities in room temperature devices as taught in column 1, lines 33 – 35.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Zubrzycki and form the grating by etching access vias through the second semiconductor layer to expose the dielectric diffraction regions and etching away the diffraction region material to define the diffraction regions out of air for the benefit of producing nanocivities in room temperature devices as taught by Scherer in column 1, lines 33 – 35.

With respect to claims 9 – 12, the limitations have been described earlier in rejecting claims 1 – 7.

Regarding claims 13 – 15, the limitations have been described earlier in rejecting claims 1 – 8.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1 – 5 and 7 – 10 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 11 of U.S. Patent No. 6,649,439.

Although the conflicting claims are not identical, they are not patentably distinct from each other because the claims 1 and 3 patented claims teach the process of growing a first semiconductor layer on a semiconductor substrate said first semiconductor layer being made of semiconductor material having an index of refraction, depositing a dielectric layer on the first semiconductor layer; patterning and etching the layer to form openings in the layer to expose selective areas on the first semiconductor layer and to create diffraction regions made out of the material; and growing a second semiconductor layer by an epitaxial growth process on the first semiconductor layer between the diffraction regions. Claims 4 and 5 teach that the nature of the semiconductor material to be either same or different.

10. Claims 5, 6 and 11 – 15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 - 11 of U.S. Patent No. 6.649,439 in view of the APA, Zubrzycki, US 6,365,428 and Scherer, US 6,468,823.

Regarding these claims 1 - 11 of U.S. Patent No. 6.649,439 fail to teach growing a third semiconductor layer of a different material with higher index of refraction.

The APA teaches the benefit of having semiconductor materials of different refractive indices and Zubrzycki and Scherer teach methods for making diffraction gratings out of semiconductor materials wherein they use a third semiconductor material

different from that of the first semiconductor material as was described earlier in rejecting the claims with prior arts.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify the teachings of claims 1 - 11 of U.S. Patent No. 6.649,439 and form the grating by depositing a third layer so that high contrast grating structures with a novel fabrication techniques can be manufactured as taught by Zubrzycki and Scherer.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar

Asok K. Sarkar
April 9, 2004

Patent Examiner